Level-3/DAQ Simulation Status Update

Gordon Watts
4-25-97
General Upgrade
Trigger Meeting

- Progress
- Plans

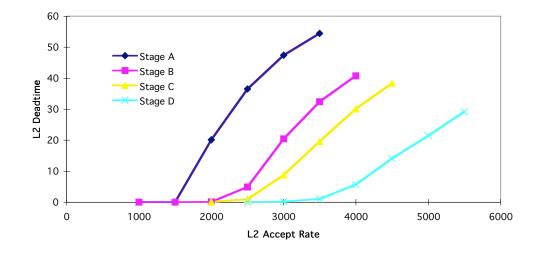
You can find all of this talk on WWW:

http://d0sgi0.fnal.gov/gwatts/talks/

Stage C and D

• Looked at Stage C and D.

	A	В	\mathbf{C}	D
Collectors	8	8	8	12
MCH Segments	16	16	16	24
L3 Segments	2	3	4	4
DC per Segment	4	16 3 4 48	4	6
L3 Nodes	48	48	64	64
50% Trigger Rate (kHz)	0.8	1.2	1.6	2.4



Mike Fortner's Crate List

- List is about a year old.
- 57 Crates
- 8 Collectors
- 162 kB/event, instead of 250 kB/event
 - Continue to use a 250 kB list for simulations.
- Crate size widths:
 - -SVX Crates: 20% (JW)
 - Other Crates: 40%
 - Widths are not correlated by detector.

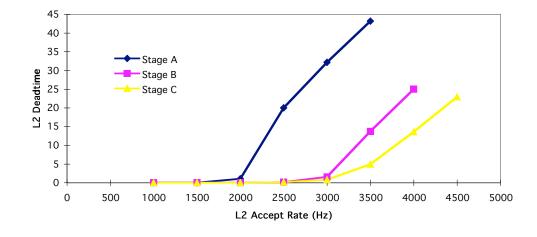
The New and the Old

Deadtime Appears (kHz):

Stage	Old List	New List
A	1.5	1.7
\mathbf{B}	2.0	2.5
${f C}$	2.5	2.8
D	3.5	N/A

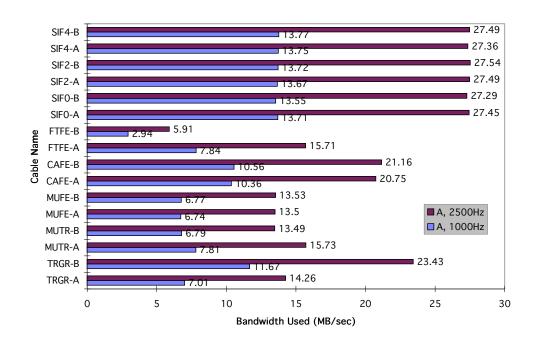
• N/A because I didn't design a crate list with Stage D's 12 collectors.

All three stages for the new crate list:



MCH Data Cable Usage

- Individual cable usage
- Stage A
- 1000 Hz and 2500 Hz L2 accept rate.
- 48 MB/sec is the limit.



• How we load the cables also depends upon geographic location of FECs.

Recent Additions

This is all preliminary

- Better simulation of CAL crates
 - Wait till L2 Accept to start digitization
 - Slow VME backplane speed (14 MB/sec)

Could easily become the limiting factor

- Clusters of crates
 - Muon crates fluctuate in unison
 - Widths of up to 40% the average

Only small effects seen in deadtime.

Plans

- I've started writing a update simulation DØNote.
- Want to study Marvin's proposed SVX/SFI crate layout better.
- Get a better handle on crates and event size.
- Simulation of path to host system.
- Better simulation of data flow in a L3 node
- Recirculation error simulation